

What is claimed are:

1. A variable gain amplifier, comprising:
 - a first means for first and second differential input voltages;
 - a second means for controlling its transconductance to generate an output current, according to a control voltage;
 - a third means for a bias current by current mirror, and to supply a stabilized bias current to the second means using the replica current; and
 - a fourth means for generating an output voltage with a variable gain according to control voltage by its output current generated in the second means.
2. The variable gain amplifier as claimed in claim 1, wherein the first means comprises:
 - a first NMOS transistor driven by the first input voltage; and
 - a second NMOS transistor driven by the second input voltage,wherein source terminals of the first and second NMOS transistors are interconnected.
3. The variable gain amplifier as claimed in claim 1, wherein the second means comprises first and second NMOS transistors connected between the first means and the fourth means, and the transconductance of each of the first and second NMOS transistors is controlled by the control voltage.
4. The variable gain amplifier as claimed in claim 1, wherein

the third means comprises:

- a current mirror for supplying a given current;

- a first PMOS transistor driven by the bias voltage, for supplying the current from the current source;

- a second PMOS transistor driven by the control voltage, for supplying the current from the current source;

- first and second NMOS transistors each connected between the second means and the ground terminal and driven by the current supplied through the first PMOS transistor; and

- third and fourth NMOS transistors connected in parallel between the first means and the ground terminal and driven by the current supplied through the second PMOS transistor.

5. The variable gain amplifier as claimed in claim 1, wherein the fourth means is a resistor.

6. The variable gain amplifier as claimed in claim 1, wherein the fourth means comprises:

- a PMOS transistor connected between a power supply terminal and an output terminal and driven by the potential of a first node;

- a NMOS transistor connected between the output terminal and the first node and driven by the output terminal; and

- a capacitor and a current source each connected in parallel between the first node and the ground terminal.

7. A variable gain amplifier, comprising:

first and second NMOS transistors driven by first and second input voltages, respectively, wherein one terminal of each of the first and second NMOS transistors is commonly connected;

third and fourth NMOS transistors connected to the first and second NMOS transistor, respectively, wherein a transconductance of each of the third and fourth NMOS transistors is controlled by a control voltage to generate various output currents;

first and second loads for generating output voltages having variable gains depending on the currents outputted through the third and fourth NMOS transistors;

a current source for supplying a given current;

a first PMOS transistor driven by a bias voltage, for supplying the current from the current source;

a second PMOS transistor driven by the control voltage, for supplying the current from the current source;

fifth and sixth NMOS transistors connected between a connecting point of the first and third NMOS transistors and a ground terminal and between a connecting point of the second and fourth NMOS transistors and the ground terminal, respectively, and driven by the current supplied through the first PMOS transistor; and

seventh and eighth NMOS transistors connected in parallel between the connecting point of the first and second NMOS transistors and the

ground terminal and driven by the current supplied through the second PMOS transistor.

8. The variable gain amplifier as claimed in claim 7, wherein each of the first and second loads is a resistor.

9. The variable gain amplifier as claimed in claim 7, wherein each of the first and second loads comprises:

a PMOS transistor connected between a power supply terminal and an output terminal and driven by the potential of a first node;

a NMOS transistor connected between the output terminal and the first node and driven by the potential of the output terminal; and

a capacitor and a current source each connected in parallel between the first node and the ground terminal.